HEWLETT PACKARD

Input/Output Instruction Group, I/O Channel, and I/O Extender Diagnostic

Reference Manual

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CONTENTS

ILLUSTRATIONS

TABLES

SECTION I
INTRODUCTION

1-1. GENERAL

This diagnostic tests the following Hardware features on HP 1000 M/E/F-Series Computer*:

a. Input/Output instructions

b. Interrupt priority structure in mainframe and/or I/O extender

c. Interrupt capability of any of the I/O slots

d. I/O channel address and I/O bus signals on any I/O slots

e. Central interrupt register

f. Overflow register

g. Switch register

h. SC02 and 03 of DCPC if present

i. Preset function

j. I/O bus switch on the HP 12979B dual port I/O extender

k. DMA transfer via a redundant (CPU or 12979B extender) system

This diagnostic operates in any HP 1000 series computer with a minimum of 8K of memory. It is one of the HP 1000 series computer system diagnostics executed in conjunction with the HP 1000 Computer Systems Diagnostic Configurator. Communication to the operator is provided through the console, if available, through the computer Memory Data Register (T-register), and the A- and B-registers. Operator input is made via the switch register and/or console.

This diagnostic assumes that the following HP 1000 series diagnostics have been successfully executed:

Alter-skip Instruction Diagnostic

Memory Reference Instruction Diagnostic

Shift-rotate Instructions Diagnostic

Memory Diagnostic

*Except where otherwise noted, when the HP 1000 M/E/F-Series is mentioned in this manual, it includes the 21MX, 21MX M-Series, 21MX E-Series, HP 1000 M-Series, HP 1000 E-Series, HP 1000 F-Series Computers and also applies to the 2100 A/S Computer. It does not include or apply to the HP 1000 A/L Series Computer.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. An HP 1000 Series Computer with at least 8K of memory. (Two HP 1000 Series Computers may be required if TEST 08-09 is to be run.) See Note 2 (below).

b. At least one, preferably several of the interface cards listed in table 1-1① are required if TEST 00-07 will be executed. These cards have to be in working condition. For redundant system see note ②. Each of the interfaces has circuit jumpers that can be installed in different positions, according to the specific application of the card. The normal installation positions for those jumpers are described in the *Operating and Service Manual* for the particular card. However, when this diagnostic program is used, some of the normal jumper installations may have to be changed temporarily while the tests are run. At the end of the diagnostic they must be returned to the position required by the specific application. The various jumper installations allowed for the diagnostic tests are listed in appendix A of this manual. Note that TEST 08 and 09 allow fewer jumper combinations than TESTS 00-07.

c. The appropriate test connector must be installed on all interface cards that are to be employed with this diagnostic. Table 1-1 lists the required test connector for each of the interface cards.

d. One or two 12979B extenders if TEST 08-09 is to be run (see note ②.)

e. If TESTS 00-07 are to be executed any interface boards compatible with HP 2100 Series Computers may be used to fill the SC's for maintaining the priority chain if the first SC to be tested is >10. Priority jumper boards 02116-6110 or 02116-8110 will suffice.

f. A diagnostic input device used only for loading the configurator and the diagnostic.

g. A console device with interface for message reporting (recommended but not required).

h. When utilizing a HP 12930A Universal Interface board, a 12777A Priority Jumper Card is required if it is not the last board (lowest priority, highest select code) in the I/O structure.

① If the installation and Service manual of any one interface board, to be used with this diagnostic, excludes a specific computer type as non-compatible with the board such statement also applies to the diagnostic.

② If TEST 08-09 will be run one interface board as listed in Table 1-1 and one 12979B I/O extender will be required if a system with redundant CPUs has to be tested. If a system has redundant extenders one HP 1000 Series Computer, two 12979B extenders and two interface boards are needed. Note that only 12979B extenders can be connected to HP 1000 Series Computers to exercise tests 08/09.

Table 1-1. Interface Boards and Test Connectors

INTERFACE BOARD		TEST CONNECTOR
NO.	NAME*	
HP 12554A	16 Bit Duplex Register Positive Logic	Part no. 1251-0332 (supplied with board).
HP 12554A-001	16 Bit Duplex Register Negative Logic	
HP 12566B/C	Microcircuit Interface Ground True	
HP 12566B/C-001	Microcircuit Interface Ground True, Party Line	Part no. 1251-0332 (supplied with board). The user has to modify that test connector by connecting pin Z,22 to pin AA,23 via a solder joint as shown in Appendix B figure B-1.
HP 12566B/C-001	Microcircuit Interface Positive True	
HP 12653A	Microcircuit Interface Special 2767A Line Printer Interface	
HP 12930A	Universal Interface Bit Differential Driver	Part no. 12930-60013 (supplied with standard board 12930A).
HP 12930A-001	Universal Interface Bit Ground True Driver	Part no. 12930-60014 (supplied with ground true board 12930A-001).
HP 12930A-002	Universal Interface Kit Positive True Driver	Part no. 12930-60015 (supplied with positive true board 12930A-002).

*Additional restrictions regarding jumper settings, type of interface board and revision code of the board are listed as a function of the tests executed in Appendix A.

1-3. REQUIRED SOFTWARE

The following software is required:

a. The Diagnostic Configurator (part numbers listed below) is used for equipment configuration and as a console device driver.

Binary	object tape	Part No. 24296-60001
Manual		Part No. 02100-90157

b. Input/output instruction group and channel/extender diagnostic binary object tape Part No. 24318-16001.

The Diagnostic Serial Number (DSN) for this diagnostic resides in memory location 126 (octal). The DSN is 141203 (octal).

NOTE

S-REG and Switch Register, P-REG and P-register, etc., used in this manual are synonymous.

PROGRAM ORGANIZATION

SECTION II

2-1. ORGANIZATION

This diagnostic consists of an Initialization and Control section and 10 tests. The Initialization and Control section accepts the select codes of the interface boards and options required by the tests. The diagnostic is divided into 2 major sections: The first one consists of tests 00 through tests 07 and tests the I/O instructions, priority structure, interrupt, channel address and bus signals, central interrupt register, overflow register, switch register, SC 02 and 03 of DCPC and the preset switch. The second section consists of test 08 and test 09 which tests the I/O bus switch on a HP 12979B dual port I/O extender connected to one or two HP 1000 Series Computer.

During the configuration of the diagnostic the operator selects either the first section (test 00-07) by clearing S-Reg. bit 15 or the second section (test 08 and 09) by setting S-Reg bit 15 (see table 3-1). It is not possible to run both diagnostic sections sequentially without reconfiguring the diagnostic.

2-2. FIRST DIAGNOSTIC SECTION (TEST 00-07)

Due to the fact that this diagnostic section verifies the proper operation of the channel address and bus signals and the priority interrupt structure it requires at least one interface board with the appropriate test connector as shown in table 1-1. If several interface boards with test connectors are available several sequential I/O channels can be tested in one diagnostic pass.

The jumpers on each interface board must be set to any one of the specified settings shown in appendix A, tables A-1, A-3, A-5 or A-7. Note, that the purpose of this diagnostic is not to test the interface board as such but the I/O instruction group and the I/O struction of the main frame and/or the I/O extender. Hardware problems on an interface board may however lead very likely to a diagnostic error. To test the interface board employ the General Purpose Register Diagnostic, part no. 24391-16001 within manual, part no. 24391-90001.

If several interface boards with test connectors are available to test the I/O structure, any combination of board types (as long as listed in table 1-1), and any number of boards can be employed. The interface boards must however occupy sequential select codes and the priority chain cannot be bridged with 12777A, Priority Jumper Cards, within the specified select code bracket. This bracket is specified during the configuration of the diagnostic (see figure 3-6 and table 3-1).

If only one select code is specified each test is configured to this select code prior to its execution. If two select codes are specified (bracket) each test is configured to the first select code specified prior to its execution, then the select code is incremented by 1, followed by a reconfiguration and re-execution of the test. This process is repeated until the test has been performed on the upper select code specified. Then the next test is entered.

Be aware that any one of the three 12930 Universal Interface boards occupies two select codes (data channel →SC XX and control channel →SC XX+1). Therefore this board must be succeeded by a 12777A, Priority Jumper Card in the next higher slot if more interface boards follow to fill all slots up to the upper select code specified. If the Universal Interface board is the last one (highest select code, lowest priority) in a specified bracket a Priority Jumper Card is not required but the next slot must be left empty. (See diagnostic limitations, paragraph 2-9, concerning utilization of control channel on a 12930 Universal Interface board.)

The specified diagnostic select code bracket can start and terminate anywhere in the mainframe or an I/O extender and can even proceed from the mainframe into the I/O extender as long as each sequential channel is occupied by a legitimate interface board (see table 1-1) and the priority chain to the beginning of the specified bracket is maintained with any jumper boards or interface boards compatible with HP 1000 Series systems (see paragraph 1-2.d) without overloading the power supply.

When a HP 12979B I/O extender is used to run test 00 through 07 the extender must be connected and configured via the switches A1S1 through A1S3 as a non-redundant system (see paragraph 3-1.a). The tests in the first diagnostic section are named as follows:

Flag test (on interrupt and interface board(s))	—	TEST 00
Overflow register test	—	TEST 01
Interrupt test	—	TEST 02
Select code screen test	—	TEST 03
Data transfer test	—	TEST 04
S-Register test	—	TEST 05
Preset test	—	TEST 06
Control register test	—	TEST 07

2-3. SECOND DIAGNOSTIC SECTION (TEST 08 AND 09)

This section is used exclusively to test the switching capabilities of the HP 12979B I/O extender(s) connected to one or two HP 1000 Series Computer(s). Contrary to the tests described in the previous paragraphs these tests are executed only on one select code in the extender(s). It is not necessary to maintain the priority chain.

Each extender to be tested must have one slot occupied by any one of the specified interface boards (see table 1-1) and its test connector. The jumpers have to be set to any one of the specified settings shown in appendix A, tables A-2, A-4, A-6, or A-8. Of all the possible configurations mentioned in the installation and service manual of the HP 12979B extender this diagnostic tests only two basic setups as described in paragraphs 2-4 and 2-5. The requirements and restrictions imposed on testing DCPC in the extender(s) is covered in paragraph 2-6.

2-4. REDUNDANT CPU's. In this set up two redundant CPU's are connected to one extender. Each CPU has control over the extender by the four I/O instructions controlling the switch in the extender. Figure 2-1-a shows the basic block diagram of a system with redundant CPU's. I/O extensions to this basic configuration can still be tested as long as the added extenders are not employed as additional switches. Figures 2-1-b and 2-1-c show testable configurations. Note that the configurator and the diagnostic must be loaded into each of the

two redundant CPU's. It is recommended that this is achieved via a diagnostic input device which is not connected to the 12979B extender. If this is not possible the extender must first be locked to port A (A1S3-switch No. 7) to load configurator and diagnostic into CPU #1, then locked to port B (A1S3-switch No. 6) to load both programs into CPU #2. Then both switches must be set to the unlocked position before the execution of the diagnostic is started.

When a console device for message reporting is connected to a CPU it cannot be shared via a common select code in the switchable extender, because the CPU(s) must have access to its console at all times during the test. During the configuration of the diagnostic the operator specifies that a CPU redundant system has to be tested by clearing S-register bit 14. (See table 3-1.)

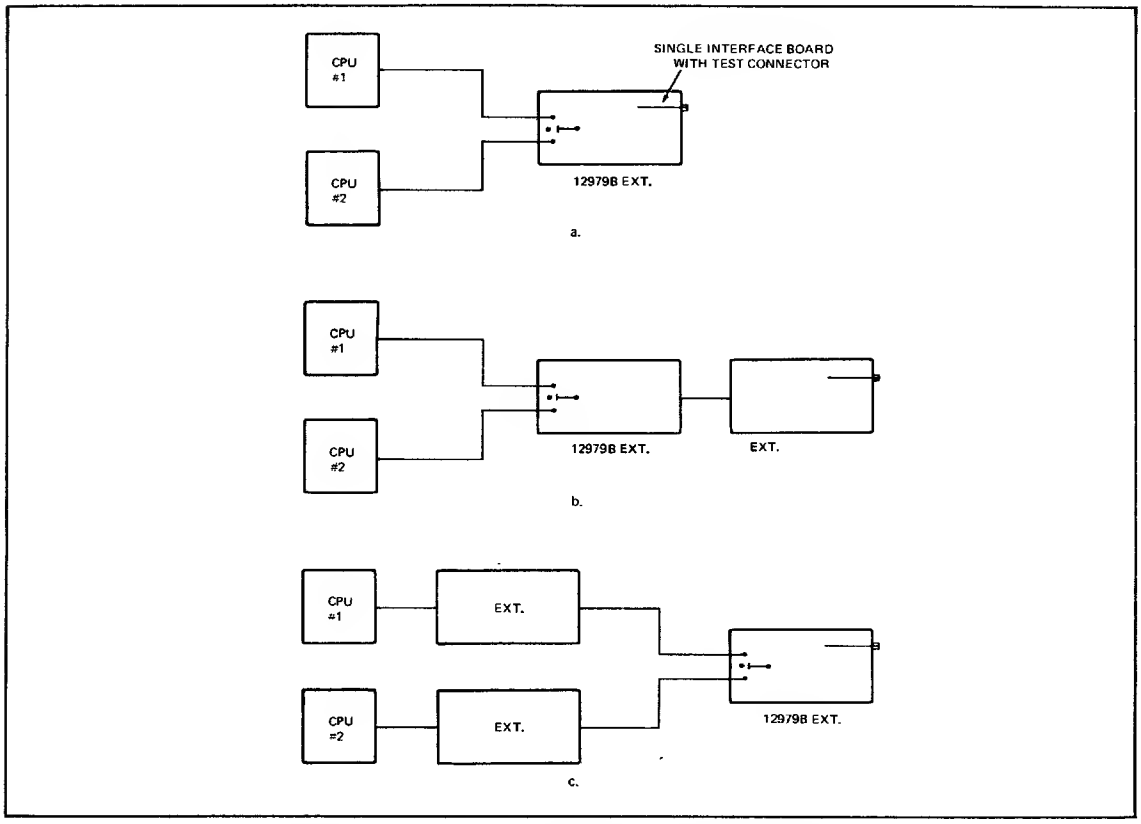


Figure 2-1. Systems With Redundant CPU's

2-5. REDUNDANT EXTENDERS. In this set up two redundant extenders are connected to one CPU which switches between either one of the two extenders and communicates to its interface board. Consider the fact that with this setup it is not possible to test the unconnected port on each extender. Figure 2-2-a shows the basic block diagram of a system with redundant extenders. I/O extensions to this basic configuration can still be tested as long as the added extenders are not employed as additional switches. Figure 2-2-b and 2-2-c show testable configurations.

It is recommended that the configurator and the diagnostic are not loaded into the CPU from a diagnostic input device which is connected to either one of the two extenders. If this is not possible, the extender, to which the diagnostic input device is connected, must first be locked to the port, via which the extender is connected to the CPU (A1S3-switch 6 or 7). Then the switch must be set back to the unlocked position before the execution of the diagnostic is started.

When a console device for message reporting is connected to the CPU it cannot interface via either one of the two switchable extenders because the CPU must have access to the console at all times during the test.

During the configuration of the diagnostic the operator specifies that a system with redundant extenders has to be tested by setting S-register bit 14. (See table 3-1.)

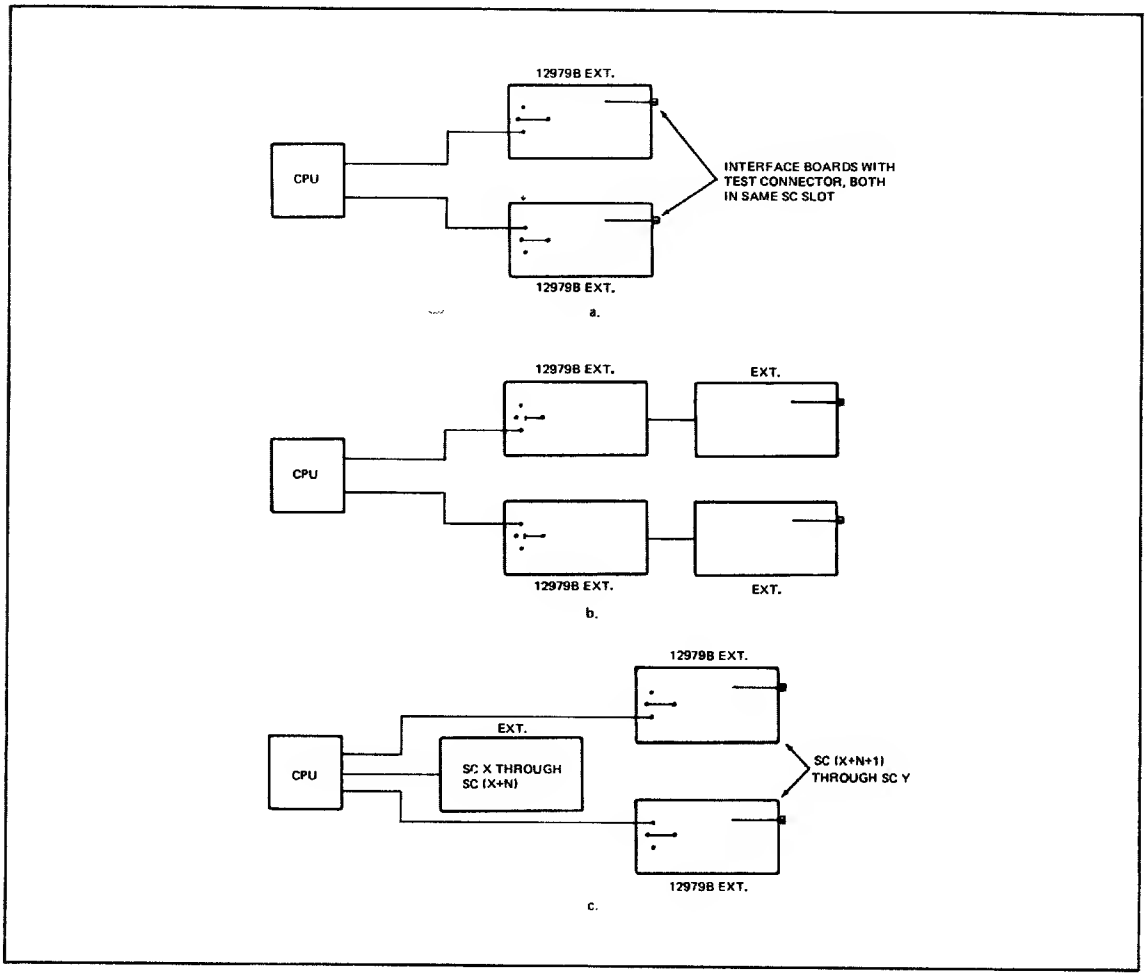


Figure 2-2. Systems With Redundant Extenders

2-6. DCPC REQUIREMENTS AND RESTRICTIONS. The DCPC board options (12898-60001) installed in the HP 12979B extender(s) will be tested with test 09. This requires of course that DCPC is installed in the CPU. During the configuration of the configurator the presence of DCPC in the CPU will be determined either automatically or manually. The presence of the DCPC board option in the extender cannot be determined automatically. Therefore the operator must specify during the configuration of the diagnostic that the DCPC board option is installed in the extender via S-register bit 13. (See table 3-1.)

2-7. TEST CONTROL AND EXECUTION

If the first diagnostic section has been selected the diagnostic outputs a title message to the console device and then executes the tests according to the options selected on the Switch Register. If the second diagnostic section has been selected the diagnostic outputs two title messages to the console device and then executes TESTS 08 and 09. The diagnostic control section primarily checks Switch Register bits 15, 13, and 12.

The diagnostic also keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if Switch Register bit 10 is clear). The count will be reset only if the diagnostic is restarted.

In the first diagnostic section, tests are executed one after the other in each diagnostic pass. User selection or default will determine which tests will be executed. Switch Register bit 9 is used to indicate that test selection is desired. (Refer to paragraph 3-3.)

By setting Switch Register bit 8 TESTS 05 and 06 will be suppressed.

When Switch Register bit 12 is set the tests that are selected will be repeated and TESTS 05 and 06 will be skipped. (See table 3-2.)

Table 2-1 shows the approximate execution time of each test on an HP 1000 M-Series Computer. The execution time will be less on an HP 1000 E/F-Series Computer.

Table 2-1. Approximate Execution Time of Each Test on an HP 1000 M-Series Computer

TEST NO.	EXECUTION TIME IN SEC
00	<0.5 sec
01	<0.5 sec
02	<0.5 sec
03	<0.5 sec
04	28 sec (Testing S-Reg, both DMA channels and 1 interface board)
05	At least 14 sec, depends on operator response
06	At least 3 sec, depends on operator response
07	<0.5 sec
08	<30 sec if redundant CPU's. / <0.5 sec if redundant extenders
09	<25 sec if redundant CPU's. / <0.5 sec if redundant extenders

2-8. MESSAGE REPORTING

There are two types of messages output for this diagnostic: error and information. Error messages are used to inform the operator when the interface fails to respond to a given control or sequence. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform an operation related to a function of the interface. In the latter case, an associated halt may occur to allow the operator time to perform the function. The operator must then press RUN. If a console device is used, the printed message will be preceded by the letter E (error) or the letter H (information) and a number (in octal). The number is also related to the halt code when a console device is not available. Examples of error and information messages are as follows: (Specific meanings are listed in section IV.)

Example — Error with halt

Message: E026 CARD IN SC XX DID NOT REPLY W FLAG
Halt Code: 102026 (octal) (T-register or Memory Data Register)

Example — Information with halt

Message: H024 PRESS PRESET (EXT & INT), RUN
Halt Code: 102024 (octal)

Example — Information only

Message: H060 12979B EXTENDER TEST WITH REDUNDANT CPU's
BUS SWITCH SC1 = XX
Halt Code: None

Error messages can be suppressed by setting Switch Register bit 11 and error halts can be suppressed by setting Switch Register bit 14. This is useful when looping on a single section that has several errors.

Information messages are suppressed by setting Switch Register bit 10. (See table 3-2.)

2-9. DIAGNOSTIC LIMITATIONS

Interface capability for receiving, passing, and denying priority (priority string logic) is not completely checked by this diagnostic. If the interface does not receive priority (i.e., PRH from the next lower select code) an error E016 NO INTRPT F SC XX will occur, with XX = the first SC specified during configuration of the diagnostic. To check this, remove some of the jumper or interface boards which are used to maintain the priority string (see paragraph 1-2.d), move the interface board(s) which is(are) employed for the actual test (see paragraph 1-2.b) down to lower SC(s), reconfigure the diagnostic accordingly and run the test again.

This diagnostic is not designed to test the interface board(s) but problems on an interface board may lead to a diagnostic failure. To test the board use the General Purpose register diagnostic no. 24391-16001.

If the HP 12930 universal interface board is used to execute the first test section (tests 00-07) the control channel (second channel) of the board can be employed on all tests. However test 04 will fail with error E031 because the control channel utilizes only six bits, the data transfer however is tested on all 16 bits. To continue, press RUN.

This diagnostic is not designed to test DMA/DCPC. However data transfers to and from SC 02 and 03 (word count registers) are executed if DMA is installed, which may lead to a diagnostic failure with error E031 and/or E032 and E042.

The diagnostic does not check the power control cable, part no. 12979-60025 on 12979B I/O extenders.

OPERATING PROCEDURES

3-1. OPERATING PROCEDURE

3-2. EXECUTING TEST 00-07

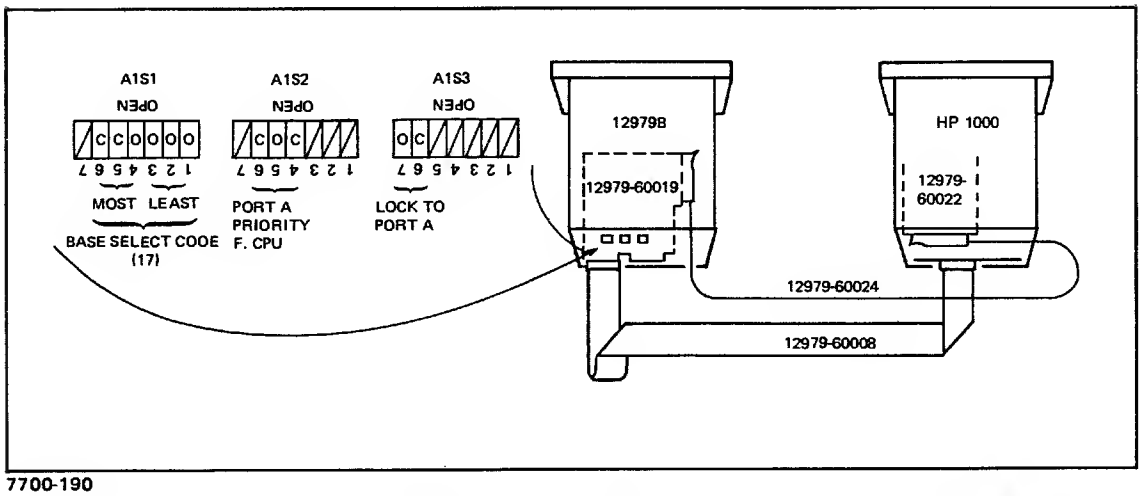
If the first diagnostic section (test 00-07) is to be executed get the available interface boards and their test connectors as specified in table 1-1, set the jumpers to any configuration specified for the appropriate board in appendix A tables A1, A3, A5 or A7 and install the boards in consecutive select code slots. If HP 12930 Universal Interface boards are used for testing, the slot with the next higher select code must be occupied by a priority jumper PCA if additional interface boards will be installed in higher select codes.

If an I/O extender is attached for testing its select codes and priorities, it must be configured as a true I/O extender, not as a redundant I/O system (applies only if the extender is a 12979B). If test 02 will be executed the priority chain must be maintained by any interface boards (jumper boards) compatible with the HP 1000 Series Computers without overloading the power supply.

Figures 3-1, 3-2 and 3-3 show the cable set up and switch settings required in case of HP 12979B extenders. The other I/O extenders (HP 2155A, HP 12979A) which do not have switching capabilities are connected to the CPU in their standard way as specified in the appropriate installation and service manual. To execute tests 00-07 proceed to paragraph 3-4.

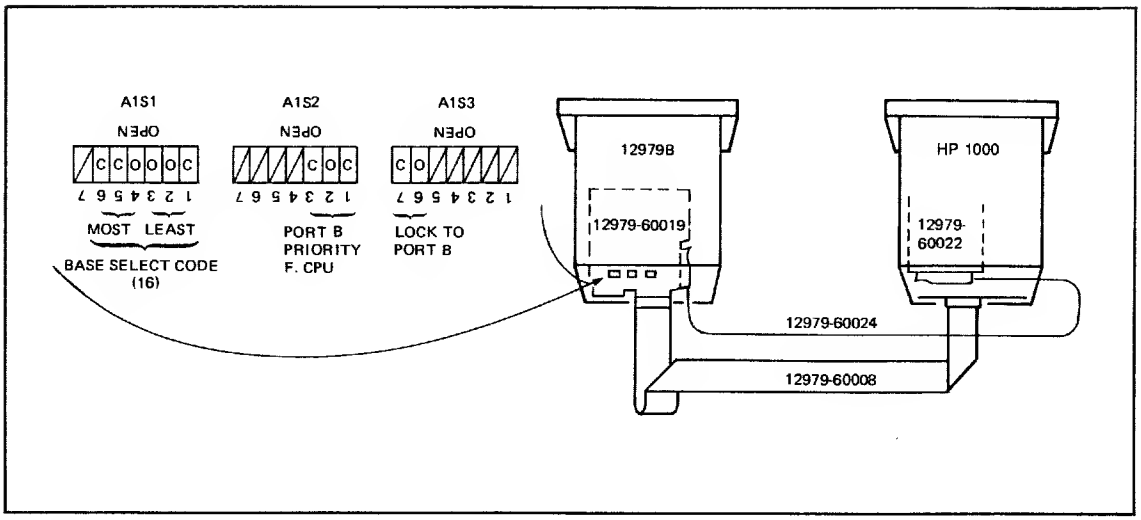
NOTE

An open switch (O) indicates a binary "one", a closed switch (C) indicates a binary "zero". The indicated base selected codes are shown as examples only. A switch shown with a line (/) indicates a no care condition.



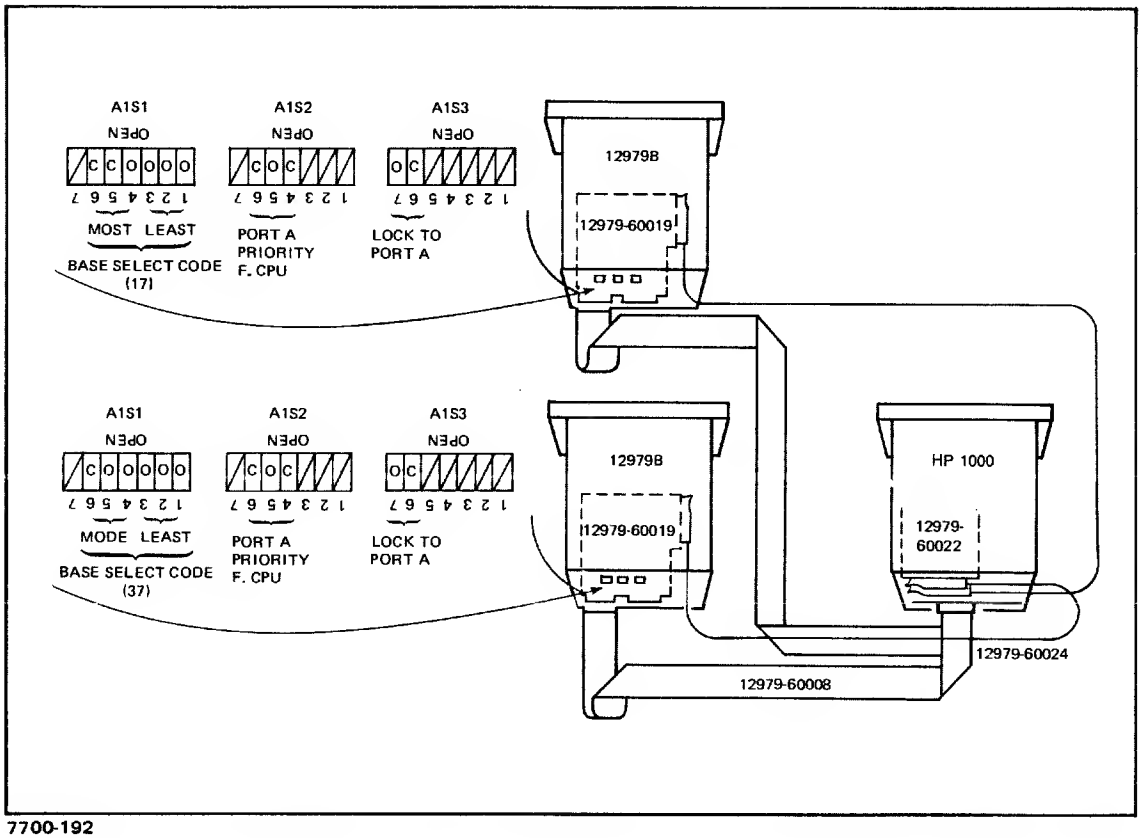
7700-190

Figure 3-1. One CPU, One Extender Connected Via Port A, Base Select Code 17



7700-191

Figure 3-2. One CPU, One Extender Connected Via Port B, Base Select Code 16



7700-192

Figure 3-3. One CPU, Two Extenders, Both Port A, Second Extender for Additional I/O

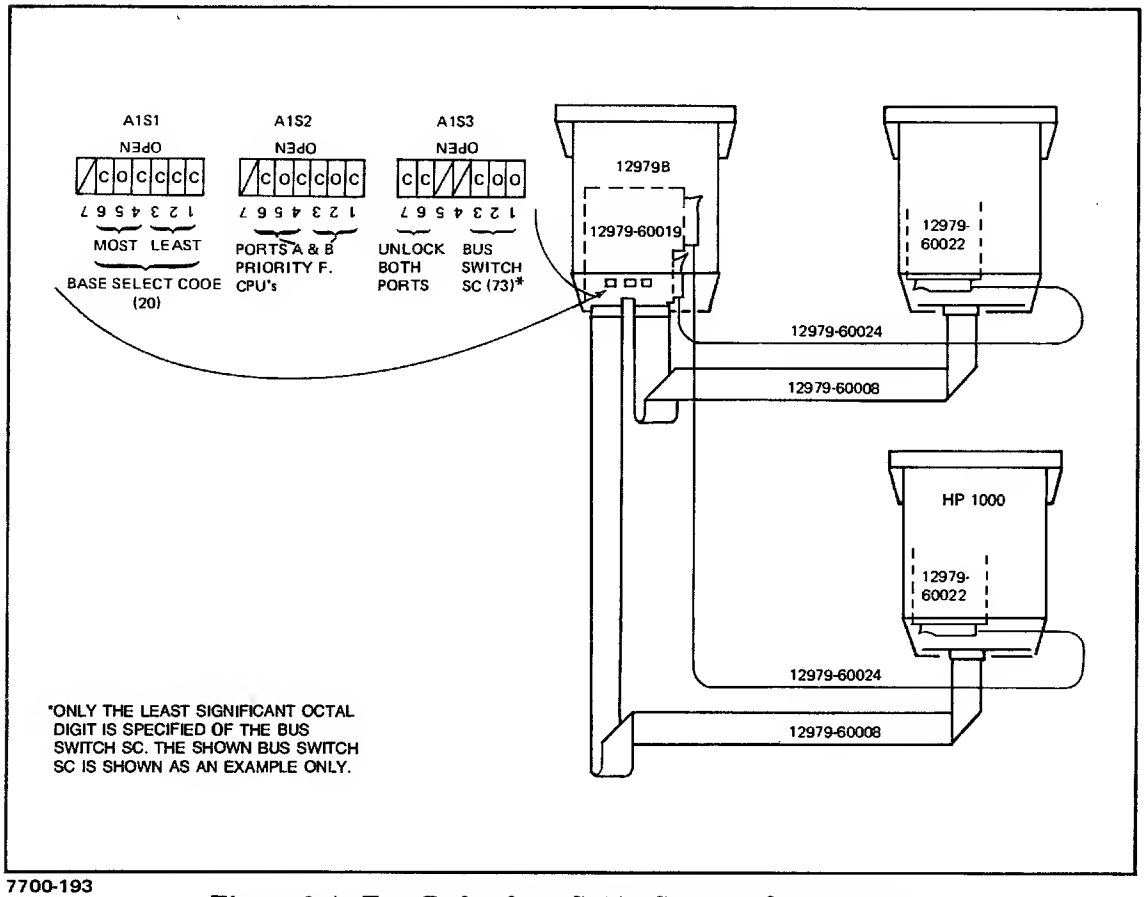
3-3. EXECUTING TEST 08 AND 09

If the second diagnostic section (test 08 and 09) is to be executed and a system with redundant CPU's has to be tested get one interface board and its test connector. If a system with redundant extenders has to be tested get two interface boards with test connectors. Set the jumpers on the board(s) to any configurations specified for the particular board in appendix A table A-2, A-4, A-6, or A-8.

Figure 3-4 shows the cable setup and switch settings required on the HP 12979B extender when tested as a system with redundant CPU's. Install the interface board with test connector into the select code on which the test shall be performed. The Diagnostic Configurator and the diagnostic must be loaded into both CPU's.

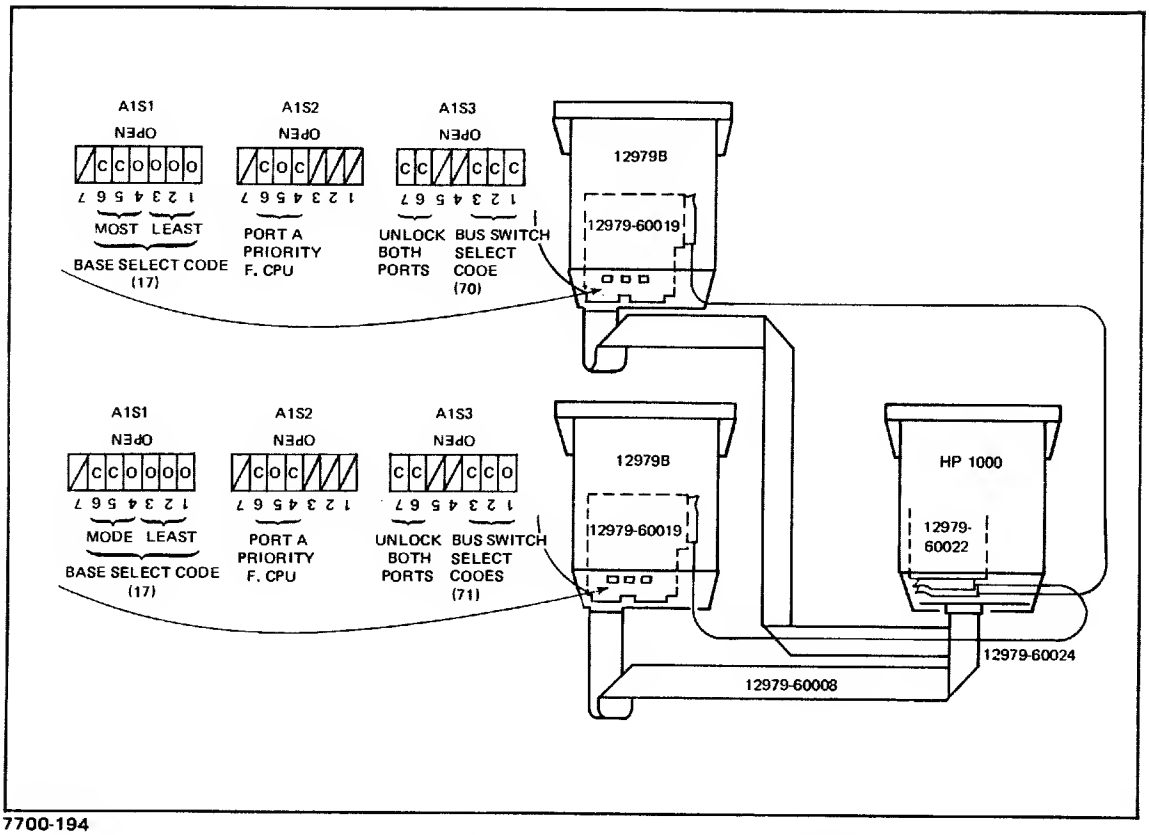
Figure 3-5 shows the cable setup and switch settings required on the HP 12979B extenders when tested as a system with redundant extenders. Install one interface board with test connector in each extender into the select code on which the test shall be performed.

To execute tests 08-09 proceed to paragraph 3-4.c.



7700-193

Figure 3-4. Two Redundant CPU's Sharing One Extender



7700-194

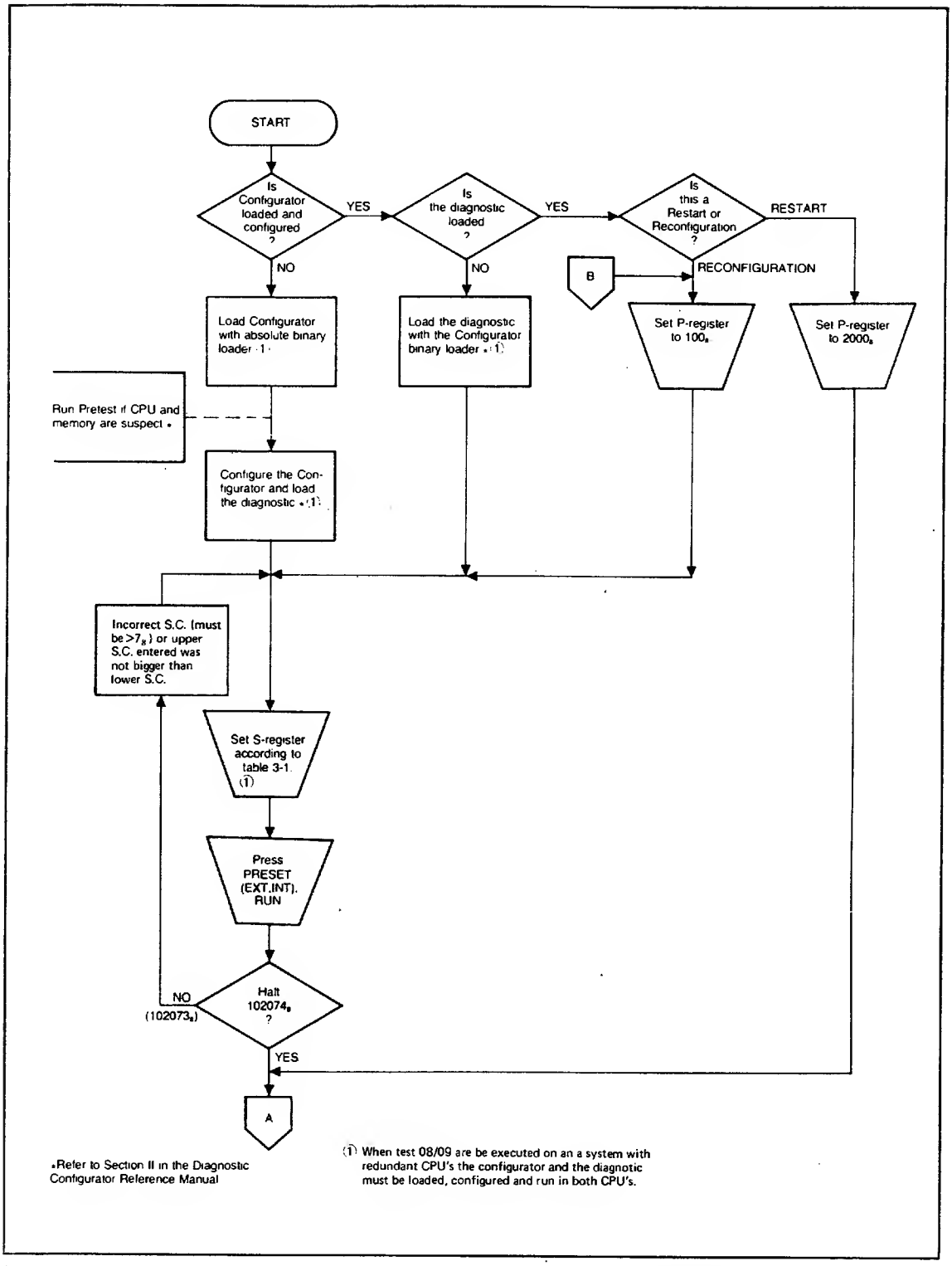
Figure 3-5. One CPU, Two Redundant Extenders Both Connected Via Port A

NOTE

An open switch ([O]) indicates a binary "one", a closed switch ([C]) indicates a binary "zero". The indicated base select codes and bus switch select codes are shown as examples only. A switch shown with a line ([/]) indicates a no care condition.

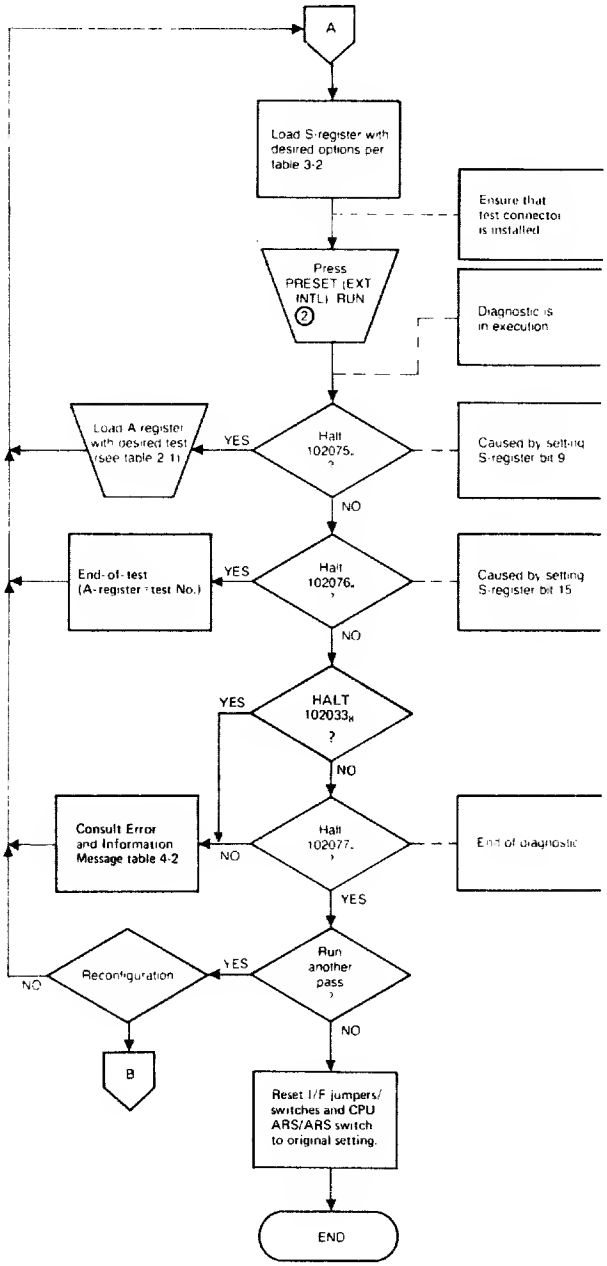
3-4. OPERATION

A flowchart of the operating procedures for loading the Diagnostic Configurator and this diagnostic is provided in figure 3-6.



7700 43

Figure 3-6. Operating Procedure Flowchart (Sheet 1 of 2)



② When test 08/09 are to be executed on a system with redundant CPU's "RUN" must be pressed on both CPU's, within less than 5 sec, else E044 followed by E043 will be reached

7700-44A

Figure 3-6. Operating Procedure Flowchart (Sheet 2 of 2)

Table 3-1. Select Codes and Diagnostic Selection

SET S-REG BITS		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
If first test section (tests 00-07) is to be selected	If several interface boards are available for testing	0	0	0	0	Set to select code of last (lowest priority) interface board installed						Set to select code of first (highest priority) interface board installed					
	If one interface board is available for testing	0	0	0	0	0	0	0	0	0	0	Set to select code of single interface board installed					
If second test section (test 08-09) is to be selected	If system with two redundant CPU's sharing one extender	1	0	Set if DMA option installed in extender (12898-60001)		Not used			Set to bus switch select code* (A1S3 switch no. 1-3 in extender)			Set to select code of interface board installed in extender					
	If system with two redundant extenders conn. to one CPU	1	1		Not used	Set to bus switch select code of extender 2* (A1S3-SW1-3)			Set to bus switch select code of extender 1* (A1S3-SW1-3)			Set to common select code of the 2 interface boards installed in both extenders					

*Bus switch select codes lay between 70_8 and 77_8. Enter in S-reg bit 6-8 (and 9-11) only the least significant octal digit of the bus switch select code. The most significant octal digit 7 will be automatically added during the configuration of the diagnostic.

Table 3-2. Switch Register Options

BIT	MEANING IF SET
0 1 2 3 4 5 6 7	Reserved
8	Suppress tests requiring operator intervention.
9	Abort current diagnostic execution at the end of the current test, and halt (102075); the user may specify a new group of tests in the A-register (see table 3-3) and press RUN.
10	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests which do not require operator intervention after diagnostic run has completed without halting. Message "PASS XXXXXX" will be output before looping unless bit 10 is set or a console device is not present. Also, TESTS 05 and 06 will be suppressed. All other selected tests in the selected test section (TEST 00-07 or TESTS 08-09) will be executed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (102076) at the end of each test; the A-register will contain the test number in octal.

Table 3-3. Test Selection Summary via A-Register

A-REG BIT	IF SET WILL EXECUTE	TEST NO.	IF DURING DIAGN. CONFIG. S-REG BIT 15 (TABLE 3-1) WAS
0	Flag test on interrupt and interface board	00	CLEARED
1	Overflow register test	01	
2	Interrupt test	02	
3	Select code screen test	03	
4	Data transfer test	04	
5	S-reg test	05	
6	Preset test	06	
7	Control register test	07	
8	12979B extender switch test	08	SET
9	12979B extender DMA (12898) test	09	

3-5. RUNNING THE DIAGNOSTIC

At the completion of each pass of the diagnostic, the pass count is output to the console. If Switch Register bit 12 was not set, the computer will halt with 102077 in the Memory Data Register (T-register). At this point the A-register contains the pass count. The operator can press RUN to execute another pass.

If bit 12 is set it causes the diagnostic to loop on the selected tests. Bit 13, when set, is used to loop on a given test that is running at the time, as specified in table 3-2. Bit 15, if set, will halt the computer at the completion of a test (Halt 102076).

If a trap cell halt occurs (106077) the operator must determine the cause of either the interrupt or the transfer of control to the location shown in the M-REG. The program may need to be reloaded to continue.

When a halt occurs and/or a message is printed on the console device, the operator must refer to table 4-2 for the meaning of the halt.

The execution time of the diagnostic is dependent upon the computer used, the card under test, the test selection and operator response time. Table 2-1 lists the approximate execution time for each test minus the time required by the operator.

3-6. TEST SELECTION

The control portion of the program provides the operator with a method to select a single test or sequence of tests to be run within the selected diagnostic section (TEST 00-07 or TEST 08-09). The operator sets Switch Register bit 9 to indicate that a selection is desired. If the computer is halted press RUN. The computer will come to a halt 102075 (octal) to indicate ready for selection (see table 3-3). If the diagnostic is running, the test in progress will be completed, then the program will halt. After the halt, the operator may load the A-register with the test selections. Bit 0 of the A-register represents Test 00, bit 1 represents Test 01, and

so on through bit 9, which represents Test 09 (decimal). The operator can only select any bit combination between 0-7 or 8-9 depending on the configuration of the diagnostic (see table 3-1, bit 15). After pressing RUN, the operator-selected test(s) will be executed. If the operator clears all bits of the A-register, all applicable tests defined in table 3-3 will be executed.

3-7. RESTARTING

The diagnostic may be restarted by setting the P-REG to 2000, loading the S-REG with the desired diagnostic options per table 3-2, then pressing PRESET (EXTERNAL and INTERNAL) and RUN.

The diagnostic may be reconfigured by setting the P-REG to 100, loading the S-REG according to table 3-1, (reconfiguring the switches A1S1-A1S3 if HP 12979B Extender testing is involved and change the cabling) pressing PRESET (INTERNAL and EXTERNAL) and RUN.

DIAGNOSTIC PERFORMANCE

SECTION IV

4-1. TEST DESCRIPTION

Tests 00 through 09 (decimal) are described below. Refer to table 4-2 (comments on halt codes) for additional details on the content of each test.

4-2. FLAG TEST, TST 00

Checks the ability to clear, set, and test the interrupt system. The following instruction combinations are tested:

```
CLF 0 - SFC 0       turn interrupt on & check
CLF 0 - SFS 0
STF 0 - SFC 0       turn interrupt off & check
STF 0 - SFS 0
```

Then some of the above instructions are modified by setting bit 11 and the routine repeated. Next the SFC and SFS instructions are modified to SFC,C and SFS,C followed by another repetition of the routine. At this point all I/O instructions are reconfigured to SC 01 and the test repeated as explained above checking therefore the overflow register. Next all I/O instructions are reconfigured to the first interface board SC and the test repeated checking the flag on the first interface board.

If several interface boards have been installed and configured the process is repeated on all interface boards. Errors in the above sequence produce error messages E000 through E003 with the machine code of the failing instructions being displayed in octal.

4-3. OVERFLOW REGISTER TEST, TST 01

This test is divided into two sections:

The first section tests the correct setting of the overflow register by executing ADA, ADB, INA and INB instructions. In the case of the first two positive as well as negative overflow is tested.

The second section tests the correct setting or clearing of the overflow register by executing the pertinent extended arithmetic (EAU) instructions which modify the overflow register if EAU capabilities are present. The overflow register should be set by an ASL instruction with overflow, a DIV instruction with the dividend too big or the divisor = 0. The overflow register should be cleared by MPY, ARS or ALS with no overflow. Error messages E004 - E012 will occur if problems with the overflow register are encountered.

4-4. INTERRUPT TEST, TST 02

This test is divided into four routines:

The first one checks that the interface board does not cause an interrupt with the flag and control set and the interrupt system turned off. The sequence of instructions is shown below:

```
STF SC      turn on board flag & control
STC SC
STF 0       turn interrupt system on & immediately off
CLF 0
```

The second routine checks that the interrupt occurred where expected with the correct return address and that no second interrupt occurred. The interrupt should not occur before a string of priority affecting instructions are executed. The following instructions are executed to check the hold off of the interrupt:

```
STC SC      turn on board flag & control
STF SC
STF 0       turn interrupt system on
STC 1
STF 1
CLC 1       interrupt should be
CLF 1       inhibited (I/O instr &
JMP *+1,I   JMP I & JSB I)
DEF *+1
JSB *+1,I
DEF *+1
NOP         interrupt should occur here
```

The third routine checks that with the interrupt system on and the interface board flag and control set there is no interrupt following a CLC SC instruction nor following a CLC 0.

The last routine checks the STC SC,C instruction on the interface board.

If several interface boards have been installed and configured the process is repeated on all interface boards. Error messages E013 - E023 and E025 - E027 will occur if problems with the interrupt system are detected.

Note that this test requires that the priority chain is not interrupted by an empty SC even below the select code bracket specified during configuration of the diagnostic (see table 3-1).

4-5. SELECT CODE SCREEN TEST, TST 03

This test checks that the Flag FF of the interface board under test is not set when STF instructions are issued to all other select codes. If several interface boards have been installed and configured the process is repeated on all interface boards. Error message E030 will occur if problems with the select code screen test are detected.

4-6. DATA TRANSFER TEST, TST 04

This test checks the OTA/B, LIA/B and MIA/B instructions on select codes 01 (S-register) if the CPU is not a 2115 or 2116, select codes 02 and 03 if DMA is installed (if the CPU is a 2114B the test is only exercised on select code 02), and on all select codes where interface boards are installed and configured. All possible combination of data patterns are transmitted, read back

and compared with the expected value on select codes 1, 2, 3 and the first interface board. On all other interface boards installed and configured the following four data patterns will be transferred: 000000, 177777, 125252 and 052525. Error messages E031 and E032 will occur if problems with the data transfer test are detected.

4-7. S-REGISTER TEST, TST 05

This test checks the manual intervention to the S-register. The diagnostic will halt twice with H033 requesting the operator to enter a predefined, alternating bit pattern into the S-register. Error message E034 will be encountered if problems with TEST 05 are detected. At the end of the test the original diagnostic options (see table 3-2) residing in the S-register, prior to entering this test, will be restored if the CPU is not a 2115 or 2116. In the other case the halt H035 will be encountered to give the operator the opportunity to restore the diagnostic options. The test will be omitted if bit 8 or 12 were set when the diagnostic options were entered (see table 3-2).

4-8. PRESET TEST, TST 06

Checks that the PRESET (EXTERNAL and INTERNAL as applicable) switch(es) on the operator panel performs the following actions: (Error messages E036 through E041 can occur.)

Sets the interface flag
Clears interface control
Turns off the interrupt system
Clears the I/O data lines
Clears the data register in the interface

The test will be omitted if bit 8 or 12 were set when the diagnostic options were entered (see table 3-2).

4-9. CONTROL REGISTER TEST, TST 07

This test checks the CLF instruction (bit 9) concatenated with MIA/B, LIA/B and OTA/B. The MIA/B, LIA/B and OTA/B instructions are not tested here (see TEST 04). The test is executed on select code 01 (overflow register), and the first interface board specified. Error message E042 will be encountered if the test fails.

4-10. 12979B I/O EXTENDER SWITCH TEST, TST 08

This test checks the special switching capabilities of either one 12979B extender under program control of two CPU's (redundant CPU's), or two 12979B extenders under program control of one CPU (redundant extenders). During configuration of the diagnostic this test will be selected with the help of S-register bit 15 (see table 3-1). According to the condition of S-register bit 14, which will specify if a system with redundant CPU's or redundant extenders has to be tested, the diagnostic will branch into either one of two major routines.

If the system consists of one CPU controlling two redundant extenders the routine will check that the CPU can switch each extender correctly with the four I/O bus switch instructions. Due to the fact that each extender is connected to the CPU only via one of the two available ports (port A or B) the proper functioning of the unused port in each extender can not be tested. If the second port must be tested it will be necessary to switch the cables part no. 12979-60008 and 12979-60024 to the untested port, assure that the switches A1S2 on both extenders are set to allow port priority from the CPU and the diagnostic executed a second time. This routine will first check that both extenders can be disconnected from the CPU, then test the four instructions on the first extender, exercise undefined I/O instructions with the SC of the bus switch of the first extender and verify that these instructions do not modify the switch setting. Then the routine is reconfigured and the test repeated on the second extender.

If the system consists of two CPU's controlling one extender it is necessary that the diagnostics residing in each of the two CPU's synchronize their activities. Because the extender is not capable of providing a status word to the two CPU's the diagnostic execution in one CPU has to resort to a synchronization — switch setting/test — wait mode, while the one in the other CPU employs a synchronization — wait — test mode. To facilitate these two different operating modes and be able to distinguish between time out and error detection of the diagnostic the operator must put both CPU's into the run mode in <5 seconds. The routines verify that each CPU can switch the extender correctly. Error messages E043 - E052 or E055 - E056 will be reached when TEST 08 fails.

4-11. DMA TEST ON 12979B EXTENDER, TST 09

This test performs a quick check on DMA in switchable 12979B extender(s). This test is automatically executed if TEST 08 was also selected via S-register bit 15 during the configuration of the diagnostic (see table 3-1), bit 13 was set to indicate that the 12898-60001 DMA option is installed in the extender and the CPU has DMA. The test requires one of the two hardware setups specified for TEST 08 (see paragraph 4-10), redundant CPU's or redundant extenders. According to the condition of S-register bit 14, the diagnostic will branch into either one of two major routines. In both routines it is assumed that the four I/O instructions which switch the extender(s) work correctly (have been checked in TEST 08).

If the system consists of one CPU controlling two redundant extenders the routine will check that the CPU can perform over each DMA channel of the first extender a successful 2-word DMA output transfer. After data verification a 2-word DMA input transfer on both DMA channels is performed. After switching to the second extender the process is repeated. Again as explained in paragraph 4-10 the unused port of each extender will not be tested.

If the system consists of two redundant CPU's controlling one extender, synchronization of the program activities in each CPU is necessary as explained in paragraph 4-10. The routines verify that each CPU is able to perform on each DMA channel a 2-word DMA output transfer followed by a 2-word DMA input transfer. Error messages E045, E052 - E055 or E057 will be reached when TEST 09 fails.

4-12. ERROR INFORMATION MESSAGES/HALT CODES

A halt code summary appears in table 4-1. Complete explanations of individual error and information messages and halt codes appear in table 4-2.

Table 4-1. Halt Code Summary

HALT	MEANING
TEST 00 (DECIMAL) THROUGH 09 (DECIMAL)	
102000 thru 102061	Error (E) or information (H) messages 00 thru 61 (octal).
CONTROL	
102073	Select code input error.
102074	End of Configuration (select code valid).
102075	User selection request.
102076	End of Test (A-register contains test number).
102077	End of diagnostic run.
106077	Trap cell halt in locations 2 thru 77 (octal).
Note: For any other halts refer to the *Diagnostic Configurator Reference Manual.*	

Table 4-2. Error and Information Messages and Halt Codes

HALT* CODE	TEST SECTION	MESSAGE	COMMENTS
NONE	Test Control	I/O INSTRUCTION GROUP AND CHANNEL OR EXTENDER DIAGNOSTIC DSN XXXXXX	Introductory message with DSN (XXXXXX = Current DSN).
NONE	Test Control	TEST XX	Information message before error message (XX equals test number). Message occurs only once within a test and is suppressed for any subsequent messages within the same test.
102000	00	E000 CLF XX SFC XX ERR YYYYYY ZZZZZZ	CLF/SFC combination failed. CLF did not clear flag or SFC caused no skip with flag clear [1] (Check if interface board installed, diagnostic correctly configured and/or I/O extender turned on).
102001	00	E001 CLF XX SFS XX ERR YYYYYY ZZZZZZ	CLF/SFS combination failed. CLF did not clear flag or SFS caused skip with flag clear.[1]
102002	00	E002 STF XX SFS XX ERR YYYYYY ZZZZZZ	STF/SFS combination failed. STF did not set flag or SFS caused no skip with flag set.[1] **
102003	00	E003 STF XX SFC XX ERR YYYYYY ZZZZZZ	STF/SFC combination failed. STF did not set flag or SFC caused skip with flag set.[1]
102004	01	E004 OV REG NOT SET BY XXX INSTR. DATA: YYYYYY ZZZZZZ	Overflow register was not set by ADA, ADB, INA or INB instruction. In case of a failing ADA or ADB instruction a 2. line is printed indicating the 2 data words added YYYYYY and ZZZZZZ which should have caused a positive or negative overflow.
102005	01	E005 ASL W. OVFW DID NOT SET OV REG	Overflow register was not set by a ASL 4 instruction and the following original values in the accumulators: B-register = 010000_8, A-register = 000000_8.

NOTE [1]: XX = SC on which test was executed:
XX = 00 → interrupt flag check failure
XX = 01 → overflow register check failure
XX ≥ 10 → flag failure on interface board
YYYYYY = machine code in octal of failing CLF/STF instruction
ZZZZZZ = machine code in octal of failing SFC/SFS instruction
A-register displays the machine code of the failing CLF/STF instruction
B-register displays the machine code of the failing SFC/SFS instruction

* Error halt codes are in octal, test numbers are in decimal.

** This halt will be reached on a 2100A/S, and HP 1000 M-Series computer with a CPU board date code 1813 or prior, displaying the E002 error twice as follows:

```
E002 STFOO SFSOO ERR
     102100 103300

E002 STFOO SFSOO ERR
     102100 107300
```

If the CPU under test will be configured with either the RTE-IVB or RTE-6/VM Operating System, a successful diagnostic pass is mandatory. To achieve this, a CPU date code of 1833 or later is required. If you are uncertain of your CPU date code, consult your local HP Sales and Service Office.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT* CODE	TEST SECTION	MESSAGE	COMMENTS
102006	01	E006 DIV W. DIVIDEND TOO BIG DID NOT SET OV REG	Overflow register was not set by a DIV instruction and the following original valves in the accumulators: B-register = 037777_8, A-register = 100000_8 and a divisor of 077777_8.
102007	01	E007 DIV BY 0 DID NOT SET OV REG	Overflow register was not set by DIV instruction with a divisor of 0.
102010	01	E010 MPY DID NOT CLEAR OV REG	Overflow register was not cleared by a MPY instruction.
102011	01	E011 ASL WITHOUT OVFW DID NOT CLEAR OV REG	Overflow register was not cleared by an ASL instruction where no overflow occurred.
102012	01	E012 ASR DID NOT CLEAR OV REG	Overflow register was not cleared by an ASR instruction.
102013	02	E013 CLF 0 DID NOT INHIBIT INTRPT ON SC XX	A CLF 0 instruction did not inhibit an interrupt from the interface board in the SC specified by XX.
102014	02	E014 INTRPT F. SC XX DURING HOLD OFF INSTR	Interrupt occurred from the interface board in the SC specified by XX while executing a JMP I, JSB I, STC, STF, CLC or CLF instruction.
102015	02	E015 SECOND INTRPT OCCURRED F. SC XX	Card interrupted a second time after initial interrupt was processed on SC XX.
102016	02	E016 NO INTRPT F SC XX	No interrupt occurred with card flag and control set on SC XX and the interrupt system on (check if test connector is installed and that the priority chain is maintained even below the low SC specified during diagnostic configuration). A-register displays the failing SC.
102017	02	E017 INTRPT RETURN ADDR ERR	Interrupt did not occur at the correct location in memory.
102020	02	E020 INTRPT EXECUTION ERR	Interrupt was not processed correctly.
102021	02	E021 CLC XX ERR	CLC instruction on SC XX did not clear card control with the interrupt system on.
102022	02	E022 CLC 0 ERR	CLC 0 instruction did not clear the card control with the interrupt system on.
102023	02	E023 CLC XX DID NOT CLEAR CONTROL FF	With Channel Control FF set and interrupt system on, a CLC to the channel still allowed an interrupt.
102024	06	H024 PRESS PRESET (EXT AND INT), RUN	Press PRESET (external and internal) then RUN.
102026	02	E026 CARD IN SC XX DID NOT REPLY W. FLAG	Card in SC XX did not reply with flag (interrupt system off). Check if board in SC XX-1 is a 12930 UI board. If so SC XX must be occupied by a jumper board.

*Error halt codes are in octal, test numbers are in decimal.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT* CODE	TEST SECTION	MESSAGE	COMMENTS
102027	02	E027 CLC XX, C DID NOT CLEAR FLAG	Flag FF in SC XX was not cleared by CLC XX,C instruction.
102030	03	E030 STF XX SET BOARD FLAG ON SC YY	A STF instruction to all SC's except SC YY set the Flag FF on the board in SC YY. XX is the SC to which the STF was issued which was responsible for the interference with SC YY. A-register = SC XX, B-register = SC YY.
102031	04	E031 OT* XX – YI* XX ERR DATA OUTPUT FROM *-REG ZZZZZZ DATA INPUT INTO *-REG VVVVVV ORIGINAL DATA IN *-REG WWWWWW	A data transfer out to and back from SC XX failed. XX = SC 01 (S-register), SC 02/03 (DMA, if installed) and all installed interface boards. * indicates the register (A/B), Y = L for LIA/B or M for MIA/B. ZZZZZZ = octal equivalent of data output. VVVVVV = octal equivalent of data received. WWWWWW = octal equivalent of original data in specified register before LIA/B or MIA/B took place. When the halt is reached the A-register will display the output data pattern, the B-register the received data pattern. Note that this halt will be reached on the command channel of every 12930 universal interface board because the command channel utilizes only IOB 15-10. Therefore the 10 least significant bits may not compare. Ignore the halt and press RUN to continue.
102032	04	E032 TIME OUT ON SC XX	Error will be encountered when the initiated data transfer to the installed interface boards is not acknowledged by a flag signal.
102033	05	H033 SET S-REG TO XXXXXX, PRESS RUN	This halt will be reached two times, first to set the octal pattern 125252, then to set the octal pattern 052525 into the S-register.
102034	05	E034 XI* FAILED FROM S-REG EXPECTED VALUE YYYYYY ACTUAL VALUE ZZZZZZ	An LIA/B or MIA/B from the S-register failed. The octal equivalent of the expected and actual values are listed. The A-register has the expected value, the B-register the actual value stored.
102035	05	H035 RESET S-REG TO DESIRED PROGR OPTIONS PRESS RUN	In case of a 2115 or 2116 computer this halt is reached to allow the operator to restore the originally selected diagnostic options.
102036	06	E036 PRESET (EXT) DID NOT SET FLAG	Preset (EXT) did not set the flag on the first interface board.
102037	06	E037 PRESET (INT) DID NOT DISABLE INTS	Preset (INT) did not disable the interrupt system.
102040	06	E040 PRESET (EXT) DID NOT CLEAR CONTROL	Preset (EXT) did not Clear Control FF on the first interface board.
102041	06	E041 PRESET (EXT) DID NOT CLEAR I/O LINES	Preset (EXT) did not clear I/O data lines.
102042	07	E042 XXX YY,C FAILED TO CLEAR FLAG	XXX indicates the I/O instruction. MIA, MIB, LIA, LIB, OTA, or OTB and YY specifies the SC of the instruction to which the CLF is concatenated whose flag did not clear. The test is performed on the overflow register and the first interface board selected.
102043	08	E043 XXX 7Y INSTR. (a....a) EXTENDER (bb)(c....c) [WITH SWITCH (d....d)]	This error messege will be encountered when any one of the 4 I/O bus switching instructions in a redundant system fail. XXX specifies the failing instruction STC, CLF, SFC or CLC. 7Y = bus switch SC of the failing instruction. (a....a) = predicate of error message. One of 4 messages will be output: a. DID NOT CONNECT b. CONNECTED c. DID NOT RELEASE d. RELEASED. (bb) specifies preposition: TO or FROM. (c....c) specifies adjective: THIS CPU or OTHER CPU. The third line is appended only when a SFC 7Y instruction failed, specifying the switch position prior to the execution of the instruction.

*Error halt codes are in octal, test numbers are in decimal.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT* CODE	TEST SECTION	MESSAGE	COMMENTS
102044	08	E044 THIS CPU TIMED OUT OR	This error message is always followed by E043 indicating that, in case of a 12979B extender connected to two CPU's, the second CPU did not respond or RUN was pressed only on one CPU.
102045	08,09	E045 FLAG FF STAYS CLEARED ON INTF.	Interface board did not reply with a flag signal.
102046	08	E046 NO SKIP ON SFC AND SWITCH IN NEUTRAL	The next instruction should have been skipped following a SFC 7X instruction.
102047	08	E047 SKIPPED ON SFC AND SWITCH ON OTHER PORT	The next instruction should not have been skipped following a SFC 7X instruction.
102050	08	E050 CPU TIMED OUT	In case of two redundant CPU's connected to one extender a time out occurred on one CPU. This error is frequently encountered if the other CPU detected an actual error E043.
102051	08	E051 XXX YY REMOVED EXTENDER FROM THIS CPU E051 XXX YY SWITCHED EXTENDER TO THIS CPU	The following 8 I/O instructions which should not cause any change to the bus switch have modified the switch setting: STF, SFS, MIA/B, LIA/B or OTA/B. XXX = the modifying instruction. YY = bus switch SC. Such an instruction may either have removed the extender or switched it to the CPU.
102052	08, 09	E052 TEST ILLEGAL ON THIS CPU	The configuration indicated the CPU is either a 2114, 2115, 2116 or 2100. The 12979B extender should not be connected to any one of these CPU's.
102053	09	E053 CPU WITHOUT DMA	Test 09 was selected during configuration of the diagnostic via S-register bit 13 but the CPU has no DMA installed.
102054	09	E054 DMA OUTPUT ERR ON BUS SW SC XX. 1/2. WORD TRANSF FAILED ON SC YY EXPECTED ZZZZZZ ACTUAL VVVVVV	A two word DMA output transferred failed. XX indicates the bus switch SC of the failing extender. The 1. or the 2. word transferred failed displaying the failing DMA SC YY = 06 or 07. The A- and B-register displayed also the expected and actual data value respectively.
102055	09	E055 DMA INPUT ERR ON BUS SW SC XX. 1/2. WORD TRANSF FAILED ON SC YY EXPECTED ZZZZZZ ACTUAL VVVVVV	A two word DMA input transfer failed. (See also explanation for E054.)
102056	08	E056 DATA TRFER ERR ON SC XX, BUS SW SC VV EXPECTED DATA YYYYYY ACTUAL DATA ZZZZZZ	A data transfer failed on SC XX indicating the interface board SC. VV indicates the bus switch SC. The expected and actual data value are also displayed in the A- and B-registers respectively.
102057	08, 09	E057 CLC XX, CLC YY DID NOT DISCONNECT BOTH EXTENDERS	In a system with redundant extenders it was not possible to disconnect both extenders from the CPU. At this point the violating extender is unknown.
NONE	Test Control	H060 12979B EXTENDER TEST WITH REDUNDANT EXTENDERS/CPU BUS SWITCH SC1 = XX SC2 = YY	Header message for 12979B extender testing (TEST 08 and 09) listing the inputted selection by the operator during diagnostic configuration (S-register bit 14) and the bus switch SC(s).

*Error halt codes are in octal, test numbers are in decimal.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT* CODE	TEST SECTION	MESSAGE	COMMENTS
102061	00-09	E061 CONFIG & TEST SEL INCOMPATIBLE	During the configuration of the diagnostic the operator has selected the 1. or 2. test section. After reaching halt 102075 to make the test selection the operator requested tests of the opposite test section. The A-Reg will display the selection made. Change the A-Reg to the correct selection and press RUN. The diagnostic will restart at the first test selected.
102073	Configuration	NONE	I/O select code(s) entered at configuration is(are) invalid. Must be greater than 7 (octal). If two select codes were entered the second one (bits 6-11) must be greater than the first one entered (bits 0-5). Re-enter valid select code(s) and press RUN.
102074	Configuration	NONE	I/O select code(s) entered at configuration is(are) valid. Enter switch register options (see table 3-2) and press RUN.
102075	Test Control	NONE	Test selection request resulting from switch register bit 9 being set. Enter the desired tests to be executed in the A-register where the bit number represents the test number. Note that any combination of bits 0 through 7 or bits 8 through 9 are valid depending on the setting of S-register bit 15 during the configuration of the diagnostic.
102076	Test Control	NONE	End of test halt resulting from switch-register bit 15 being set (A-register equals test number). To continue press RUN.
102077	Test Control	PASS XXXXXX	Diagnostic run complete. (A-register value = pass count in octal.) Switch register options may be changed. To continue, press RUN.
106077	Test Control	NONE	Halt stored in locations 2 through 77 (octal) to trap interrupts which may occur unexpectedly because of hardware malfunctions. M-register contains the I/O slot number of interrupt. Diagnostic may be partially destroyed if halt occurs. The program may have to be reloaded; the problem should be corrected before proceeding.

*Error halt codes are in octal, test numbers are in decimal.

REQUIRED JUMPER INSTALLATIONS

APPENDIX A

Each of the interface cards that can be used to test the I/O channels and extenders must have, during execution of the diagnostic, a certain combination of circuit jumper positions installed. The combinations allowed are listed below in tables A-1 through A-8, according to the type of interface card and the tests to be executed.

A-1. HP 12554A 16-BIT DUPLEX REGISTER (POSITIVE LOGIC) BOARD NO. 12554-60023

Any one of the following jumper combinations is allowed during the execution of tests 00-07. The revision code of the board is irrelevant.

Table A-1. Jumper Combination for TESTS 00-07

		Positions under Combination Number					
		1	2	3	4	5	6
Jumper Number	W4	B	B	A/B	A/B	A	A
	W5	B	A	A	B	A	B
	W6	A/B	A	C	C	A/B	A
	W7	A	A	B	A	B	B
	W8 — W12 Installed						
	*W13	A	A	A	A	A	A
	*W14	A	A	A	A	A	A

*If applicable.

Any one of the following jumper combinations is allowed during the execution of tests 08 and 09. Note that the board revision must be equal to or later than 939 with jumper W13 and W14 in positions A.

Table A-2. Jumper Combination for Test 08-09

		Position under Combination Number			
		1	2	3	4
Jumper Number	W4	B	B	A	A
	W5	B	A	A	B
	W6	A	A	A	A
	W7	A	A	B	B
	W8 — W12 Installed				
	W13	A	A	A	A
	W14	A	A	A	A

A-2. HP 12554A-001 16-BIT DUPLEX REGISTER (NEGATIVE LOGIC) BOARD NO. 12554-60024

Any one of the following jumper combinations is allowed during the execution of tests 00-07. The revision code of the board is irrevelant.

Table A-3. Jumper Combination for Tests 00-07

		Positions under Combination Number					
		1	2	3	4	5	6
Jumper Number	W4	A/B	A	A/B	A/B	A/B	B
	W5	A	A	A	B	B	A
	W6	B	A	C	C	B	A
	W7	B	B	B	A	A	A
	W8 — 12 Installed						
	*W13	A	A	A	A	A	A
	*W14	A	A	A	A	A	A

*If applicable

The following jumper combination is allowed during the execution of tests 08 and 09. Note that the board revision must be equal to or greater than 939 with jumpers W13 and W14 in positions A.

Table A-4. Jumper Combination for Test 08-09

Jumper Number	W4	B
	W5	A
	W6	A
	W7	A
	W8 — W12 Installed	
	W13	A
	W14	A

A-3. HP 12566B/C-001, HP 12566B/C-002, HP 12566B/C-003 MICROCIRCUIT INTERFACE

Any one of the following jumper combinations is allowed during the execution of tests 00-07. The revision code of the board is irrevelant.

Table A-5. Jumper Combination for Tests 00-09

JUMPER	12566B	12566C
W1	C	C
W2	B	B
W3	B	B
W4	B	B
W5	IN	OUT
W6	IN	OUT
W7	IN	OUT
W8	IN	OUT
W9	A	A
W10	NA	B
W11	NA	IN
W12	NA	OUT
W13	NA	OUT

A-7. HP 12930A UNIVERSAL INTERFACE KIT

Any of the following switch combinations is allowed during the execution of tests 00-07. The revision code of the board is irrevelant.

Table A-7. Switch Combination for Tests 00-07

Switch	Position Under Combination Number			
	1	2	3	4
85 S1	1	1	1/2	1
S2	5	5	5	5
S3	8	8	9	9
87 S1	1/2	1/2	1	1
S2	4/5	5	5	5
S3	8	8	7/8	7/8
97 S1	1	1	1	1
S2	5	4	5	5
S3	10	10	10	9
102 S1	2	2	2	2
S2	7	7	7	7
S3	10	10	10	10
106 S1	1	1	1	1
S2	5	5	5	5
S3	9	9	9	9

Any one of the following switch combinations is allowed during the execution of tests 08-09. The revision code of the board is irrevelant.

Table A-8. Switch Combination for Test 08-09

Switch	Position Under Combination Number		
	1	2	3
85 S1	1	1	1
S2	5	5	5
S3	8	8	9
87 S1	1/2	1/2	1
S2	4/5	5	5
S3	8	8	8
97 S1	1	1	1
S2	5	4	5
S3	10	10	9/10
102 S1	2	2	2
S2	7	7	7
S3	10	10	10
106 S1	1	1	1
S2	5	5	5
S3	9	9	9

TEST CONNECTIONS

APPENDIX B

Figure B-1 shows the modification required to the test connector part no. 1251-0332 to utilize the 12566B or 12653A microcircuit interface board.

PINS		SIGNAL SIGNAL
FROM	TO	
A	1	Bit 0 to Bit 0
B	2	Bit 1 to Bit 1
C	3	Bit 2 to Bit 2
D	4	Bit 3 to Bit 3
E	5	Bit 4 to Bit 4
F	6	Bit 5 to Bit 5
H	7	Bit 6 to Bit 6
J	8	Bit 7 to Bit 7
K	9	Bit 8 to Bit 8
L	10	Bit 9 to Bit 9
M	11	Bit 10 to Bit 10
N	12	Bit 11 to Bit 11
P	13	Bit 12 to Bit 12
R	14	Bit 13 to Bit 13
S	15	Bit 14 to Bit 14
T	16	Bit 15 to Bit 15
Z,22	AA,23	Device Command to Device Flag
BB	24	N/C (GROUND)

Figure B-1. Modified Test Connector No. 1251-0332

READER COMMENT SHEET

Input/Output Instruction Group,
I/O Channel, and I/O Extender Diagnostic
Reference Manual

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